1. Description

The SP001GBSDU400O02 is a 64M x 8bits Double Data Rate SDRAM high-density for DDR-400.The SP001GBSDU400O02 consists of 8pcs CMOS 64Mx8 bits Double Data Rate SDRAMs in 58 pin TSOP package, and a 2048 bits serial EEPROM on a 200-pin printed circuit board. The SP001GBSDU400O02 is a Dual In-Line Memory Module and is intended for mounting into 200-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

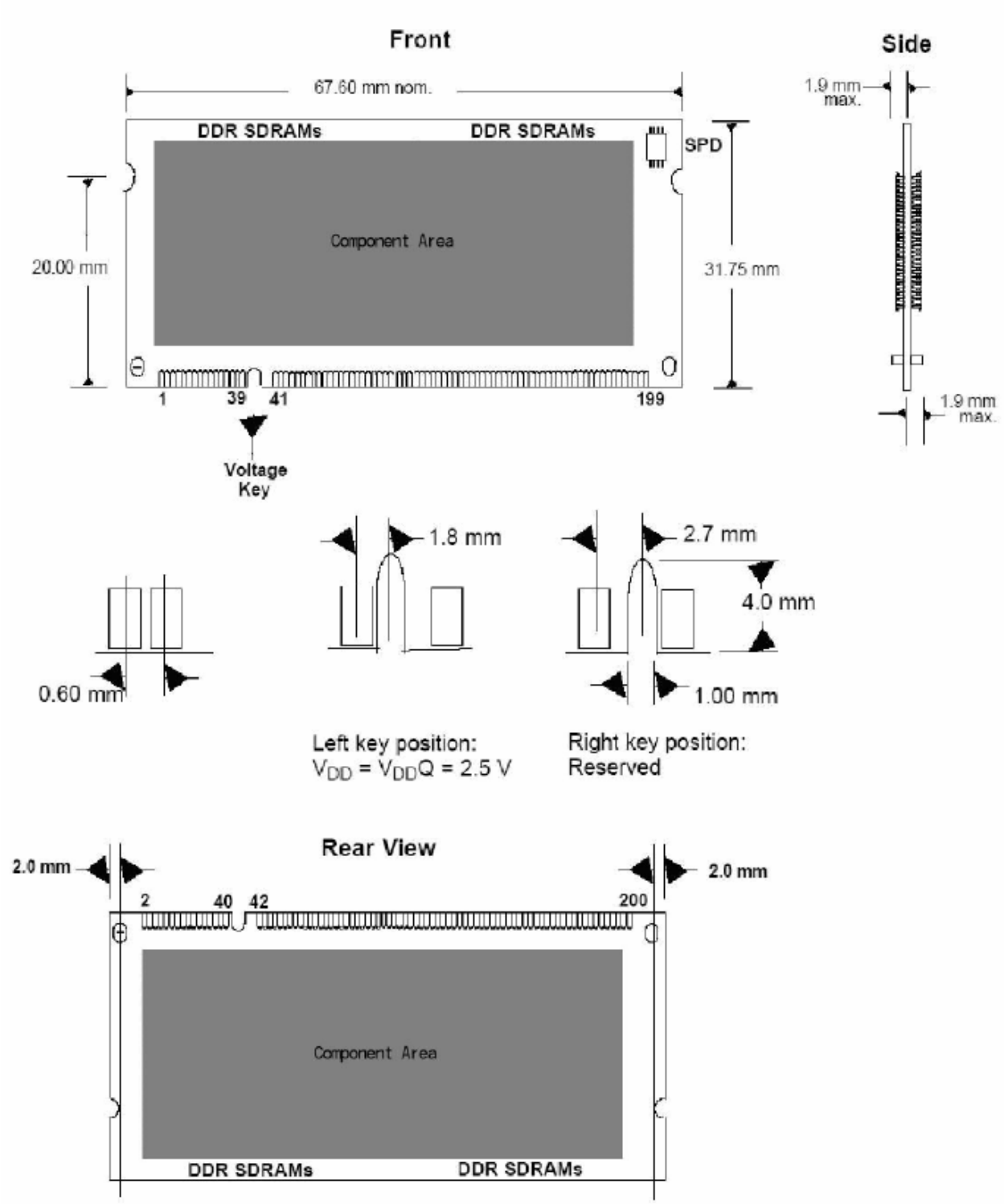
2. Features

- **Double--data--rate architecture; two data transfers per clock cycle**
- **Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver**
- **DQS is edge--aligned with data for READs; center--aligned with data for WRITEs**
- **Differential clock inputs (CK and /CK)**
- **DLL aligns DQ and DQS transitions with CK transitions**
- **Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS**
- **Four internal banks for concurrent operation**
- **Data mask (DM) for write data**
- **Burst lengths: 2, 4, or 8**
- **AUTOPRECHARGE option for each burst access**
- **Auto Refresh and Self Refresh Modes**
- **JEDEC standard 2.5 V (SSTL_2 compatible) I/O**
- **58pin TSOP II Leaded & Pb-Free (RoHS compliant) package**

3. Module Specification

Item	Specification
Capacity	1024MByte
Physical Bank(s)	2
Module Organization	128M x 64bit
Module Type	Unbuffered Non ECC
Speed Grade	PC-3200 / (DDR 400)
Voltage Interface	SSTL_2
Power Supply Voltage	2.6V±0.1V
Burst Lengths	4 or 8
DRAM Organization	64M x 8bit DDR SDRAM
PCB Layer	6Layers
Contact Tab	200 pin GOLD Flash Plating
Serial PD	Support

4. Simplified Mechanical Drawing with Keying Positions



5. Pinouts

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	VREF	**51**	VSS	**101**	A9	**151**	DQ42	**2**	VREF	**52**	VSS	**102**	A8	**152**	DQ46
3	VSS	**53**	DQ19	**103**	VSS	**153**	DQ43	**4**	VSS	**54**	DQ23	**104**	VSS	**154**	DQ47
5	DQ0	**55**	DQ24	**105**	A7	**155**	VDD	**6**	DQ4	**56**	DQ28	**106**	A6	**156**	VDD
7	DQ1	**57**	VDD	**107**	A5	**157**	VDD	**8**	DQ5	**58**	VDD	**108**	A4	**158**	/CK1
9	VDD	**59**	DQ25	**109**	A3	**159**	VSS	**10**	VDD	**60**	DQ29	**110**	A2	**160**	CK1
11	DQS0	**61**	DQS3	**111**	A1	**161**	VSS	**12**	DM0	**62**	DM3	**112**	A0	**162**	VSS
13	DQ2	**63**	VSS	**113**	VDD	**163**	DQ48	**14**	DQ6	**64**	VSS	**114**	VDD	**164**	DQ52
15	VSS	**65**	DQ26	**115**	A10/AP	**165**	DQ49	**16**	VSS	**66**	DQ30	**116**	BA1	**166**	DQ53
17	DQ3	**67**	DQ27	**117**	BA0	**167**	VDD	**18**	DQ7	**68**	DQ31	**118**	/RAS	**168**	VDD
19	DQ8	**69**	VDD	**119**	/WE	**169**	DQS6	**20**	DQ12	**70**	VDD	**120**	/CAS	**170**	DM6
21	VDD	**71**	NC	**121**	/S0	**171**	DQ50	**22**	VDD	**72**	NC	**122**	/S1	**172**	DQ54
23	DQ9	**73**	NC	**123**	NC	**173**	VSS	**24**	DQ13	**74**	NC	**124**	NC	**174**	VSS
25	DQS1	**75**	VSS	**125**	VSS	**175**	DQ51	**26**	DM1	**76**	VSS	**126**	VSS	**176**	DQ55
27	VSS	**77**	NC	**127**	DQ32	**177**	DQ56	**28**	VSS	**78**	NC	**128**	DQ36	**178**	DQ60
29	DQ10	**79**	NC	**129**	DQ33	**179**	VDD	**30**	DQ14	**80**	NC	**130**	DQ37	**180**	VDD
31	DQ11	**81**	VDD	**131**	VDD	**181**	DQ57	**32**	DQ15	**82**	VDD	**132**	VDD	**182**	DQ61
33	VDD	**83**	NC	**133**	DQS4	**183**	DQS7	**34**	VDD	**84**	NC	**134**	DM4	**184**	DM7
35	CK0	**85**	NC	**135**	DQ34	**185**	VSS	**36**	VDD	**86**	NC	**136**	DQ38	**186**	VSS
37	/CK0	**87**	VSS	**137**	VSS	**187**	DQ58	**38**	VSS	**88**	VSS	**138**	VSS	**188**	DQ62
39	VSS	**89**	CK2	**139**	DQ35	**189**	DQ59	**40**	VSS	**90**	VSS	**140**	DQ39	**190**	DQ63
41	DQ16	**91**	/CK2	**141**	DQ40	**191**	VDD	**42**	DQ20	**92**	VDD	**142**	DQ44	**192**	VDD
43	DQ17	**93**	VDD	**143**	VDD	**193**	SDA	**44**	DQ21	**94**	VDD	**144**	VDD	**194**	SA0
45	VDD	**95**	CKE1	**145**	DQ41	**195**	SCL	**46**	VDD	**96**	CKE0	**146**	DQ45	**196**	SA1
47	DQS2	**97**	NC	**147**	DQS5	**197**	V_{DDSPD}	**48**	DM2	**98**	NC	**148**	DM5	**198**	SA2
49	DQ18	**99**	A12	**149**	VSS	**199**	VDDID	**50**	DQ22	**100**	A11	**150**	VSS	**200**	NC

6. Pin Description

SYMBOL	TYPE	DESCRIPTION
CK0-CK2, /CK0-/CK2	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs and DQS /DQS) is referenced to the crossings of CK and /CK.
CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWERDOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, /CK and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought to HIGH. After CKE has been brought HIGH, it is an SSTL_2 input only.
/S0, /S1	Input	**Chip Select:** Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM0-DM7	Input	**Input Data Mask:** DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
BA0 – BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A0 - A12	Input	**Address Inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
DQ0-DQ63	Input/Output	**Data bit Input/ Output:** Bi-directional data bus.
DQS0-DQS7 /DQS0-/DQS7	Input/Output	**Data Strobe:** output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	Power supplies for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins
V_{DD}, V_{SS}	Supply	Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD} / V_{DDQ} planes on these modules.
V_{REF}	Supply	Reference voltage for SSTL 18 inputs.
SDA	Input/Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup onthe system board.
V_{DD}SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD} / V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.
SA0-SA2	Input	These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EERPOM address range
V_{DDID}		VDD Identification Flag